Amendments to the Claims

1. (Currently Amended) A method in a packet switched data transfer system for processing header bits and payload bits in a frame of bits, the method comprising:

classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits based upon a location of the header bit in the frame of bits;

classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits based upon a location of the payload bit in the frame of bits;

processing the first predetermined class of bits, in the frame, in accordance with a first predetermined mechanism; and

processing the second predetermined class of bits, in the frame, in accordance with a second predetermined mechanism.

2. (Original) The method of claim 1, further comprising:

constructing a new frame of bits based upon the processed first predetermined class of bits and the processed second predetermined class of bits.

3. (Cancelled)

4. (Currently Amended) ~~The method of claim 1, wherein:~~ A method in a packet switched data transfer system for processing header bits and payload bits in a frame of bits, the method comprising:

classifying each of the header bits in the frame into ~~the~~ a first predetermined class of bits and into ~~the~~ a second predetermined class of bits ~~includes classifying each of the header bits~~ based upon a pre-assigned header weight of the header bit; ~~, and~~

classifying each of the payload bits in the frame into ~~the~~ a first predetermined class of bits and into ~~the~~ a second predetermined class of bits ~~includes classifying each of the payload bits~~ based upon a pre-assigned payload weight of the payload bit

processing the first predetermined class of bits, in the frame, in accordance with a first predetermined mechanism; and

processing the second predetermined class of bits, in the frame, in accordance with a second predetermined mechanism.

5. (Original) The method of claim 1, wherein:

processing the first predetermined class of bits in accordance with the first predetermined mechanism includes grouping the first predetermined class of bits; and

processing the second predetermined class of bits in accordance with the second predetermined mechanism includes grouping the second predetermined class of bits.

6. (Original) The method of claim 1, further comprising:

grouping the processed first predetermined class of bits;

grouping the processed second predetermined class of bits; and

constructing a new frame of bits based upon the grouped-processed first predetermined class of bits and the grouped-processed second predetermined class of bits.

7. (Original) The method of claim 1, wherein:

the first predetermined mechanism includes applying a first error protection algorithm, and

the second predetermined mechanism includes applying a second error protection algorithm.

8. through 14. (Cancelled)

15. (Currently Amended) A packet switched data transfer device comprising:

a frame receiver configured to receive a frame of bits, the frame of bits comprising a plurality of header bits and a plurality of payload bits;

a bit classifier coupled to the frame receiver, the bit classifier configured to classify each of the plurality of header bits into a first class of bits and into a second class of bits based upon a location of the header bit in the frame of bits and each of the plurality of payload bits into a first class of bits and into a second class of bits based upon a location of the payload bit in the frame of bits; and

a bit processor coupled to the bit classifier, the bit processor configured to process the classified first class of bits, in the frame, according to a first predetermined process and to process the classified second class of bits, in the frame, according to a second predetermined process.

16. (Cancelled)

17. (Currently Amended) ~~The packet switched data transfer device of claim 15, wherein:~~ A packet switched data transfer device comprising:

a frame receiver configured to receive a frame of bits, the frame of bits comprising a plurality of header bits and a plurality of payload bits;

~~the~~ a bit classifier coupled to the frame receiver, the bit classifier ~~is further~~ configured to classify each header bit of the plurality of header bits into a first class of bits and into a second class of bits based upon a pre-assigned header weight of the header bit and to classify each payload bit of the plurality of payload bits into a first class of bits and into a second class of bits based upon a pre-assigned payload weight of the payload bit; and

a bit processor coupled to the bit classifier, the bit processor configured to process the classified first class of bits, in the frame, according to a first predetermined process and to process the classified second class of bits, in the frame, according to a second predetermined process.

18. (Original) The packet switched data transfer device of claim 15, wherein:

the first predetermined process has a first coding rate, and

the second predetermined process has a second coding rate, the second coding rate less than the first coding rate.

19. (Original) The packet switched data transfer device of claim 15, further comprising:

a frame constructor coupled to the bit processor, the frame constructor configured to construct a new frame of bits based upon the processed first class of bits and the processed second class of bits.